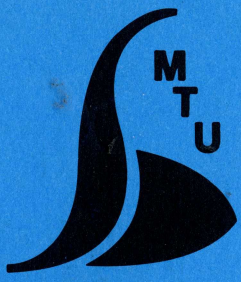


P.A.

Micro Technology Unlimited

6502 PERIPHERALS AND PRODUCTS

CATALOG A1

OCTOBER 1, 1978

MICRO TECHNOLOGY UNLIMITED
PRICE LIST

PRODUCT	DESCRIPTION	NOV. 1, 78 PRICE*	JAN. 1, 79 PRICE**
K-1000A	POWER SUPPLY ASSEMBLED	30.00	35.00
K-1002A	DAC MUSIC BOARD ASSEMBLED W/MANUAL	35.00	40.00
K-1002B	DAC BARE BOARD W/MANUAL	12.00	12.00
K-1002M	DAC MANUAL	5.00	6.00
K-1002-1L	ADVANCED MUSIC SOFTWARE ISTING	10.00	15.00
K-1002-1C	K-1002-1L WITH KIM CASSETTE	13.00	20.00
K-1005A	5 SLOT CARD FILE W/MOTHERBOARD	68.00	75.00
K-1008A	VISIBLE MEMORY ASSEMBLED W/MANUAL	238.00	240.00
K-1008B	VISIBLE MEMORY BARE BOARD W/MANUAL	40.00	42.00
K-1008M	VISIBLE MEMORY MANUAL	9.00	10.00
K-1008-1L	TEXT/GRAPHICS DISPLAY SOFTWARE LISTING	20.00	22.00
K-1008-1C	K-1008-1L WITH KIM CASSETTE	25.00	27.00
K-1012A	PROM-I/O BOARD ASSEMBLED W/MANUAL	NOV. 78	237.00
K-1012B	PROM-I/O BARE BOARD W/MANUAL	NOV. 78	42.00
K-1012M	PROM-I/O MANUAL	NOV. 78	10.00
K-1016A	16K MEMORY ASSEMBLED W/MANUAL	338.00	340.00
K-1016B	16K MEMORY BARE BOARD W/MANUAL	40.00	42.00
K-1016M	16K MEMORY MANUAL	9.00	10.00
K-1020A	PROTOTYPING BOARD ASSEMBLED	40.00	42.00

*Add $2.00 for shipping and handling within continental USA. All other shipments add $5.00. (Manual only orders add $1.00 in USA, $1.50 outside USA.)

**All prices as of January 1, 1979 include shipping in continental USA. All other shipments add $3.00. (Manual only orders outside USA add $0.50.)

NOTES:

1. PLEASE GIVE STREET ADDRESS TO ALLOW UNITED PARCEL SERVICE DELIVERY.

2. Assembled items are complete with all parts installed (except as noted on spec sheets) and are fully tested and burned in at the factory to insure that all specifications are met.

3. Outside of U.S.A. orders must be prepaid in U.S. dollars by Money Order or prior arrangements made with MTU. Foreign companies, universities, etc. please include all customs forms required for seller to fill out and where possible, name of import broker you wish to expedite shipment receipt.

MICRO TECHNOLOGY UNLIMITED

Micro Technology Unlimited (MTU) was founded to bring high technology products and technical information to the market in easy to use form. Our present implementation of this goal consists of products based around the 6502 microprocessor. Its price and performance are excellent which allow us to build sophisticated products and educational tools in the price range of budgets which earlier could not afford this kind of computing/teaching power. The principals of the company are Howard (Hal) A. Chamberlin Jr. and David B. Cox. These men have been operating together in a synergistic manner for over 10 years. Many disciplines of engineering and technology have been worked in, giving a broad-based background to work from.

The products offered in this catalog were developed from speculation by MTU with the above goal in mind. To date, no product has been offered which failed to succeed as a viable, marketable product for MTU. We work both with individuals desiring to own a versatile microcomputer, with companies who can use our products as subassemblies in their products, and with people teaching others about technology and theory.

In addition to these standard product offerings, we perform custom product design, development and production for companies or individuals who have ideas, but need the engineering expertise to create and turn those ideas into product reality. We continually are working with several companies at a time on their product problem solving. We are interested in working with anyone in almost any field who have useful ideas which we can implement or improve upon. Our designs fulfill all market requirements before we are thru - including profitability to insure success. If you have a problem that you feel electronics, optics, mechanics, packaging, etc. can be used to create a solution for, write or call us, we're interested.

ADDITIONAL INFORMATION

For more information other than specification sheets in this catalog, we suggest purchase of the manual for the product in question. This purchase will be credited toward purchase of the associated product hardware. Manuals include schematics, parts list and layout, principles of operation, troubleshooting guide, specifications, and diagnostic program listing. If the manual does not answer your questions or they are of a different nature than you feel the manual will address, please ask us and we will be happy to answer them.

WARRANTY

All products of MTU are warranted for 6 months from the date of shipment from the factory to be free from defective parts and workmanship. Any other damages including but not limited to; misuse, abuse, fire, flood, or other acts of God are not covered by this warranty. Units under warranty requiring repairs are to be returned to the factory postpaid, and will be returned postpaid within 2 weeks from date of receipt of the unit at the factory. No statements other than these printed specifications are made or implied. Liability of MTU is limited to repair or replacement of faulty unit(s) and does not extend beyond the purchase price paid for the unit(s).

SYSTEM COMPATIBILITY OF MTU PRODUCTS

KIM-bus Systems: All MTU products have been carefully optimized for ease of use with the original KIM-1. Recently, however, other manufacturers of the 6502 microprocessor IC have introduced KIM-like single board computers which for the most part emulate the fundamental KIM characteristics as well as provide significant enhancements. One of these is the SYM-1 (formerly VIM-1) from Synertek and the other is the AIM-65 from Rockwell International. Both of these boards utilize expansion and application connectors that are essentially identical to the corresponding KIM connectors. All of our products can be interfaced to these systems (referred to as "KIM-bus" systems in the product descriptions) with little or no additional effort. In some cases board dimension differences or the disposition of edge connector pins that were unused in the KIM-1 will require special consideration.

All software packages are written for direct execution on KIM-1 based systems. Since the I/O port addresses and memory arrangement is different in the other KIM-bus systems, the software packages must be patched to run successfully on the SYM or AIM. The high level of documentation supplied with all software packages greatly simplifies this task. Cassettes, when supplied, are written in standard speed KIM format and are guaranteed to be readable by a standard KIM-1. The current version of the SYM-1, although advertised as being able to read KIM format tapes, is quite sensitive to recorder differences and may not be able to read our KIM cassettes.

Other 6502 Systems: Many of our products are useful on other systems which utilize the 6502 microprocessor. Examples are the Apple II, and the PET. In particular our DAC and DAC/ADC boards may be directly connected to parallel input/output ports that may be available on the basic system or an I/O expansion. As with alternate KIM-bus systems, software will require a small amount of patching to match I/O and memory addresses.

Products designed for direct bus interface such as the Visible Memory graphic display and other memory boards can also be used if the customer is willing to bring the necessary bus signals out from the processor. Since the KIM bus is essentially the unbuffered 6502 processor bus (except for a couple of TTL inverters), virtually all of the required signals will be available right at the pins of the microprocessor.

6680 Based Systems: The DAC and DAC/ADC boards can be used directly on any 6800 based system. Bus interface boards may be connected in a manner similar to the Apple and PET however, the 6800 bus signal, VMA, must be handled. The simplest method is to AND VMA and A15 together and use the result as A15 to the MTU bus interface board. It is important that the Phase 2 clock to our memory boards not be added with VMA. Note that all software must be rewritten to run on a 6800 CPU.

The Visible memory requires a 1.0MHz system clock in order to generate correct scanning frequencies while the K-1016 is adjusted for a 1.0MHz system clock. Either board can be adjusted to synchronize to clock frequencies down to 750KHz however the non-standard scanning frequencies that result when the K-1008 is readjusted will require the use of a high quality video monitor to avoid image waver from 60Hz hum. SWTP 6800 systems, which use an 875KHz clock, can in most cases be upgraded to 1.0MHz speed by replacing the crystal thus gaining a 15% speed improvement as well as compatibility with the Visible Memory.

Systems Using Other Processors: Boards using parallel I/O such as the DAC and DAC/ADC can connect to the parallel ports of any computer. The software must however be rewritten in the machine language of the host CPU. Since the music software is speed sensitive, its capabilities may be reduced when rewritten for slower microprocessors such as the 8080 or Z-80.

Bus interface boards such as the Visible Memory will require significant interface circuitry or modification to run with other busses such as S-100. Because of the erratic bus timing of other processors, the no wait state characteristic of the boards may have to be given up.

K-1002-1 ADVANCED MUSIC SOFTWARE

The advanced music software package is a collection of several programs designed to further enhance the educational and musical value of the 6502 processor and K-1002 music board. Maximum convenience and longer songs require an additional 4K or more of memory. Programs included are as follows:

Simplified music interpreter: This interpreter is essentially the same as the one described in BYTE Magazine Sept., 1977. Musical "subroutine" (refrains) capability has been added with nesting to over 10 levels depending on stack allocation. This program runs in the basic KIM-1 memory.

Fourier series program: This program accepts a table of up to 16 harmonic amplitudes and phases and computes a 256 point waveform table usable with either the simplified music interpreter or the advanced interpreter. All arithmetic is double precision and the resultant waveform is normalized in amplitude for minimum quantization noise. A package of double precision arithmetic subroutines is part of the program. This program runs in the basic KIM-1 memory.

Advanced music interpreter: This interpreter allows a more compact and flexible song table than the simplified interpreter while retaining 4 voice capability. Each musical event requires as little as 1 byte rather than the constant 5 bytes needed by the simplified interpreter. Provisions for separate waveforms for each voice, variations in tempo, changes in timbre, and "musical subroutines" are included. The interpreter resides in 1K memory with an additional 4K recommended for song and waveform storage.

Music compiler: This program accepts an ASCII string from the teletype serial port (or other device with user supplied I/O routines) and produces interpretive code in memory for the advanced music interpreter and a printed listing. The compiler requires 2.5K of memory plus storage for interpretive song data.

The K-1002-1L is a set of fully assembled source listings which are heavily commented.

K-1005 CARD FILE AND MOTHERBOARD FOR KIM-1

The K-1005 card file was designed to answer the need for a compact quality mechanical support and electrical connection system for the KIM-1. The card file will hold up to five boards including the KIM-1. It is constructed of a black anodized aluminum frame with custom angled support for the KIM keyboard. The motherboard is supplied assembled with five connectors which are parallel wired. The topmost connector plugs onto the KIM expansion fingers and is wired with memory expansion signals and +12 volt power to the sixth connector mating with the KIM application edge fingers. There is no buffering on the motherboard, thus, it draws no power.

The KIM is mounted horizontally above the other boards with the card file top open for easy access to the keyboard and displays. The back edge of the KIM is bolted to the angled support for extra keyboard rigidity while the front plugs into the two edge connectors. The other cards are physically supported in standard, deep slot plastic card guides. The compact design with expansion boards out of the way uses minimum table space and protects the hardware.

The motherboard is double-sided, plated-through, glass-epoxy construction. It contains five standard 44 pin edge connectors and a five position terminal strip. The topmost connector is positioned to mate with the KIM's expansion edge fingers. The connectors are glass filled diallyl phythalate with bifurcated gold-plated contacts. The short bus and proper attention to shielding and grounding allows the full 4 low power Schottky load capability of the KIM-bus to be realized. The terminal strip provides power connections to the KIM (+5 and +12 volts regulated) and expansion boards (+7.5 and +16 volts unregulated).

The frame is one piece of formed 16 gage aluminum protected with a black anodize finish. A cutout space and mounting holes are provided for additional edge connectors on the application side for use with our expansion boards or other user functions. Mounting holes on both the bottom and top edges of the frame allow solid mounting to a base and installation of a cover for the KIM. Expansion boards are simply plugged in but the KIM and its support must be unbolted to remove it from the card file.

Clearance Dimensions: 11.25 inches deep, 8.5 inches wide and 4.75 inches high.

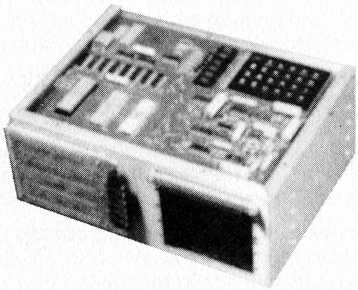
Bus: Signal pinout compatible with the standard KIM-1 expansion bus.

Connectors: 6 supplied, 5 on motherboard and 1 to mate with KIM application connector. Standard 44 pin double sided, .156" contact spacing edge finger connectors.

Power Connector: 5 position terminal strip for +7.5, +5, ground +12, and +16 volt power input. The motherboard draws no power itself.

CPU Compatability: Mechanically optimized for the KIM-1. Can be used with SYM-1 with minor modification to card file and/or SYM-1 board. Since the AIM-65 is 12" wide, it must mount outside the card file.

Card Size: 8.5 "high by 11" deep. Edge fingers equivalent to KIM-1 finger spacing from edge opposite keyboard side.



K-1008 8K MEMORY/RASTER GRAPHIC DISPLAY GENERATOR

The MTU Visible Memory is a unique concept in microcomputer memory systems. The board is an 8K memory add-on to KIM-bus systems which includes the circuitry to simultaneously display the memory contents as 64,000 dots on a TV monitor. Unlike many other add-on memory boards, this one is designed for the KIM-bus and is merely connected in parallel with the expansion connector. The processor continues to run at full speed with no wait states, no software overhead or CPU time required to refresh the display. There is no snow or other visible interference on the screen when the display memory is being accessed by the processor (or any other time). Logic on the Visible Memory automatically refreshes the display.

The basic display format is 200 lines of 320 dots per line. This format coupled with the K-1008-1 software package makes the Visible Memory an exceptionally versatile mixed text and graphics display. The high resolution graphics capabilities make interaction possible with a degree of realism never before available on a microcomputer.

Extensive use of "LS" IC's and 4K dynamic memory IC's is responsible for the low power consumption and small size of the board. Problems experienced with dynamic memory in other systems are absent in this board due to the superior bus control architecture of the 6502 processor and MTU advanced circuit design. The circuitry that generates the display pattern also refreshes the memory automatically as it scans.

The memory address can be jumper selected at any 8K boundary with the 8K memory block contiguous from the selected address. An extra jumper selectively disables the top or bottom half of the display thus allowing 4K to be used for program storage without showing up as a random pattern on the screen. The "Decode Enable" and "K7" signals needed for the KIM-1 to expand beyond 4K memory are generated by the board and need simply be connected to the proper pins of the KIM application connector. These signals are not used on the SYM and AIM processors. Up to four Visible Memory boards may be connected directly to an unbuffered KIM-bus.

For further information, order the manual (see below).

Manual: Complete hardware schematics, principles of operation, timing diagram, programming instructions, and troubleshooting guide.

Sockets: All memory chips and decode enable IC.

Display Format: 200 lines, 320 dots per line, non-interlace.

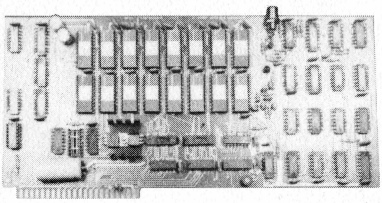
Scanning Frequencies: (derived from 1 MHz processor clock) Horizontal: 15,625 Hz, Vertical: 60.1 Hz. Required video bandwidth: 4 MHz. For 50 Hz operation, request MTU APPLICATION NOTE 3.

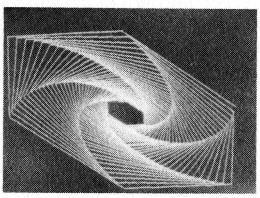
Output: 1.25 V p-p composite video into 75 ohms, sync negative.

Adjustments: dot sync (prealigned on assembled units).

Power Requirements: unregulated + 7.5V @ .25 amp, + 16V @ .25 amp. (– 5V for the memory chips is generated on board).

Size: 5" high by 11" wide exclusive of edge fingers.





K-1008-1 TEXT/GRAPHICS DISPLAY SOFTWARE

The display software package for the K-1008 Visible Memory is designed to provide the user with a library of utility display oriented subroutines written in assembly language. By incorporating calls to these routines, the user can create and manipulate text and graphic images whose complexity is limited only by the 320 by 200 display matrix size. Most routines operate on X and Y coordinate arguments stored in page 0. In addition to the subroutine library, two demonstration programs are provided.

Summary of Major Subroutines

Set pixel, clear pixel, flip pixel, write accumulator contents to pixel address, load pixel address contents to accumulator. Pixel location is at X1:Y1 coordinates.

DRAW/ERASE: Draw white lines or erase (draws black lines) a line between X1:Y1 and X2:Y2 coordinates.

PIXADR: Load to the accumulator the pixel address and bit contents of the pixel at X1:Y1 coordinate. (500 bytes for all graphic routines.)

DCHAR: Displays a character whose upper left corner is at X1:Y1 coordinate. Character code is full ASCII and matrix is 5 x 7 with lower case descenders making it effectively 5 x 9.

DTEXT: Accepts ASCII characters and formats them into text. Interprets ASCII control,codes CR, LF, BS, DC1-DC4 (cursor movement), and SI/SO (baseline shift for sub/superscript). Text starts at X1:Y1 coordinates which are updated following each call. Underline cursor at current location is provided. The font is a 5 x 9 matrix in a 6 x 11 field providing 18 lines of 53 characters, with sub/super script operation allowed on the full character set. (2500 bytes with all features, includes DCHAR.)

SDTEXT: Simplified version on DTEXT. Interprets CR, LF, BS, FF, Underline cursor provided. Uses a less sophisticated method of addressing. The font is a 5 x 7 matrix in an 6 x 9 field providing 22 lines of 53 characters. This subroutine requires less program memory to operate in than DTEXT. (1200 bytes with lower case, 1000 bytes without.)

Summary of Demonstration Programs (Run in Standard 1K byte KIM-1 memory)

LIFE: Implements the game of Life in the full 320 by 200 matrix. The KIM keyboard may be used to set the initial colony pattern and control evolution of the generations.

SWIRL: Produces an infinite variety of patterns under the control of two parameters. Uses a simple difference equation algorithm.

The subroutine package is available as commented, assembled source listings. For convenience in hand relocation (if desired), all temporary storage is done in the stack and base page and relative jumps are used where possible. Locations that must be modified when relocating are designated by underlining.

The demonstration programs reside in the standard KIM RAM and assume that the Visible Memory starts at 2000.

K-1012 PROM-I/O-PROM PROGRAMMER SYSTEM BOARD

This system oriented expansion board converts the processors into powerful yet easy to use turn-key systems. The board handles up to 12 Kbytes of 2708 PROM, four 8 bit parallel ports, a UART controlled serial port and — a 2708 PROM programmer with programming socket. The 12 Kbytes of industry standard PROM capacity is sufficient to hold Microsoft BASIC for the KIM in addition to input/output routines (such as text/graphics routines for the Visible Memory video display), or other application programs as desired. Four 8 bit parallel input/output ports with full handshaking and interrupt capability as well as a UART controlled serial port open I/O bottlenecks in expanded systems. This board may be connected directly to a KIM-bus system (1 "LS" TTL load on the bus); no modification of any kind and no external interface circuitry is required. Special signals required by the KIM-1 when memory is expanded beyond 4K (Decode Enable and K7) are generated onboard.

Although standard 2708 PROM's are utilized, the K-1012 continues the MTU tradition of low power consumption and operation from standard KIM-1 power supply voltages. Because the PROM's require - 5 volts, it is supplied onboard by a high efficiency inverter circuit. A unique power down circuit for each PROM disconnects its power when not accessed for longer than one microsecond. Because only one PROM can be accessed at a time, the total power consumption for twelve PROMs is scarcely more than that for one.

Parallel input/output is expanded to an additional 32 ports through the use of two 6520 PIA circuits. Each of the 32 ports is individually programmable as input or output. In addition, 4 pairs of handshaking control lines are available for positive verification of data transfer to and from external devices or additional I/O functions. Also 4 independently maskable interrupts, each associated with 8 I/O lines and one pair of handshaking lines, are included. This interrupt capability is fully compatible with the KIM-1 monitor or may be disabled with jumpers.

Serial input/output is provided by a type 6850 Asynchronous Communications Interface Adapter. True RS-232 with proper positive and negative output voltages is the interface method with all of the important modem control signals provided. Full maskable interrupt operation for transmitted data, received data, and modem control is provided. Standard baud rates from 75 to 4800 may be selected by plugable jumpers or user supplied dipswitch.

A 2708 PROM programmer and socket is provided as a standard feature. This socket in conjunction with two of the parallel ports (connections onboard) provides programming and verification functions. The parallel ports may be used for I/O when not actually programming a PROM. Again following MTU tradition, an on-board inverter supplies the + 26 volts needed for PROM programming.

Power Requirement: Unregulated + 7.5 volts .35 amp, + 16 volts .25 amp typical, .35 amp peak during programming.

Addressing: 8K of PROM Must be contiguous on an 8K address boundary, remaining 4K may be scattered in a second 8K block. I/O requires 16 contiguous addresses between FEOO and FEFF. Sockets provided for address jumpers.

Buffering: Maximum of 1 LS TTL load on address and data bus.

Size: 7½" high by 11" wide exclusive of edge fingers.

Manual: Contains detailed principles of operation, complete schematic, parts list and layout and loopback diagnostic and PROM programmer program listing. PROM's are not included.

K-1016 16K BYTE MEMORY BOARD

This 16K byte memory board may be connected directly to any KIM-bus processor with no modifications and no additional external interface circuitry. The K-1016 is connected in parallel with the expansion connector containing the KIM-bus signals. Special signals required by the KIM-1 when memory is expanded beyond 4K (Decode Enable and K7) are generated by the K-1016 memory board. These are available at otherwise unused expansion connector pins and are simply wired to the corresponding pins on the KIM's application connector.

The memory uses standard 22 pin dynamic memory IC's for low operation. The refreshing is totally transparent and performed by logic on the board. Refreshing is totally transparent and performed by logic on the board. Refreshing is done during Phase 1 when the processor is setting up for the next memory cycle which means that no wait states or processor overhead is required. Memory timing is precisely generated and synchronized to the 1.0mHz processor clock by means of a phase-locked loop frequency multiplier and countdown state generator.

The power consumption of the board is less than 1/5 that of typical 8K memory boards for the KIM. On-board regulators allow operation from unregulated +8 and +16 volt sources or with a simple jumper change regulated +5 and +12 volt sources. Since the memory chips require −5 volts, it is generated on-board to allow use of standard KIM power supplies which do not generate this voltage.

Access Time: The data is stable greater than 100 nanoseconds prior to fall of system phase 2 clock which latches the data bus.

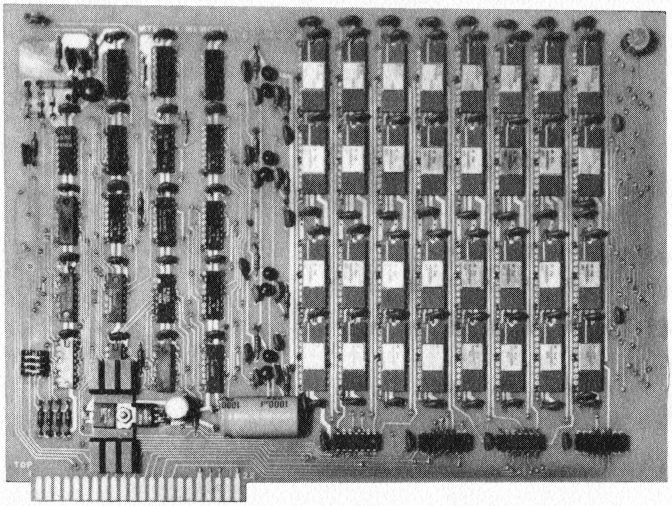
Cycle Time: Internally synchronized to 1 mHz system Phase 2 clock as used in 6502 and 6800 systems.

Buffering: Maximum of 1 LS TTL load on address and data bus.

Power requirement: unregulated +7.5V 0.2 amp, +16V 75 milliamp standby, 200 milliamp maximum with 100% access (−5V required for the memory IC's is generated. onboard).

Addressing: The 16K bytes must be contiguous but may start at any 4K boundary. A socket is provided for jumpers or user supplied dip switch for address selection.

Size: 7½" high by 11" wide exclusive of edge fingers.



K-1020 PROTOTYPING BOARD

As many of our customers have requested, we now offer a prototyping board for KIM-bus systems. It is assembled with on-board +5 Volt and +12 Volt regulators and mounts in the K-1005 card file. Both Expansion and Application edge fingers are provided with gold plating and pads for wire-wrap post or direct wiring. The board has power bussing on both sides, all holes are plated through and it is constructed of standard glass epoxy material.

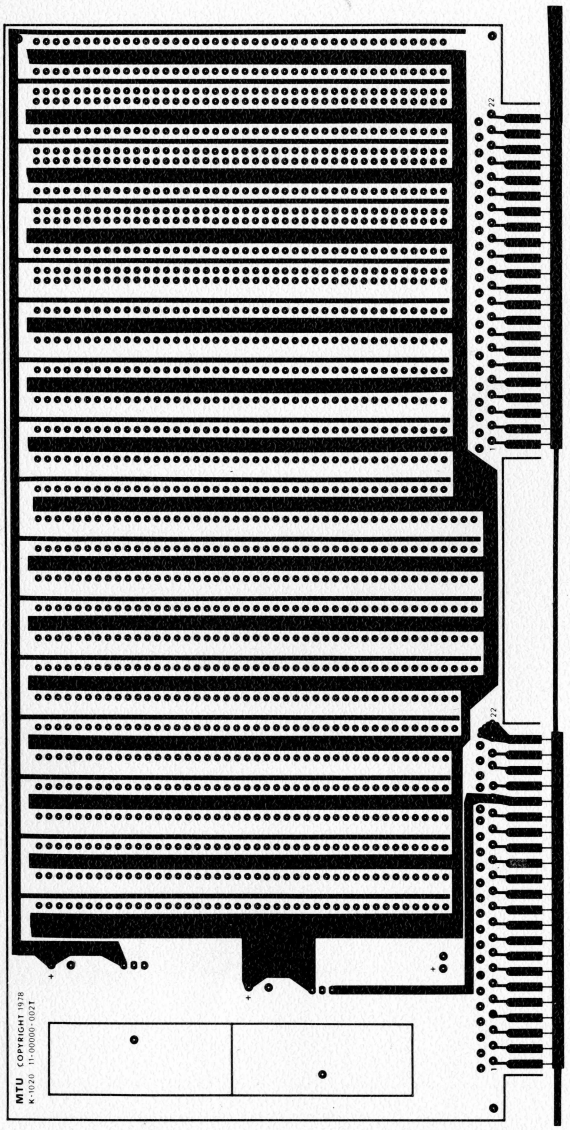
A universal hole pattern covers part of the board which allows 8, 14, 16, 18, 20, 22, 24, 28, 40 and even 64 pin IC's to be used. The maximum capacity is seventy-five, 14 and 16 pin IC's to be used. The 40 pin dips with space left for 14 smaller dips.

A heavy ground plane occupies most of the bottom side of the board while separate power planes for +5V and +12V intermesh on the top side. Bypass and input filter capacitors for the regulators are provided.

Size: 5" high by 11" wide exclusive of edge fingers.

Regulators: +5 volts 1.2 Amp, volts .250 Amp.

Inclusions: Example schematic of interface circuit to the KIM-bus, layout assembly sheets, and power schematic and pinout designations.



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